

FPGA Design Case Study – Signal Acquisition Sub-System Interface for Defense Applications

NeST successfully completed a project to design and implement a FPGA based interface sub-system for a signal processing and visualization system for a defense application. The video processing sub-system is based on TI's DaVinci SoC, and FPGA based glue logic is used to interface it to the signal processing sub-system.

NeST's Scope of Work

- Design
- RTL Development
- Verification
- HW Integration

FPGA Implementations in Video Processing Sub-System

1. B-Mode image processing
2. X-Y address generation
 - a. Acoustic Frame Memory address generation
 - b. Cordic Transformation
3. Interpolation - 480 x 128 pixels are converted to 480 x 512
4. Gray scaling using look up table
5. Video data formatting – Raw to YCbCr
6. Bus decoding

FPGA Implementations in Signal Processing Sub-System

1. Interface signal generation with required timing to interface DaVinci with ASIC
2. Dual Port RAM implementation
3. Vector averaging and frame averaging

Tools Used

- Xilinx ISE
- ModelSim (Mentor Graphics)