



Introduction

Color Enhancer IP core is a video processing core that provides a stand-alone mechanism to adjust the color properties of RGB video source. Color adjust is an inevitable feature present in almost all video processing systems ranging from consumer displays to automobile entertainment systems.

The IP core helps system designers to build this feature in FPGA based video processing systems with minimum risk. It has effectively implemented a computational technique, where the color of the input video source can be adjusted in 64 steps for gain ranging from 0 to 2.

The use of high-performance XtremeDSP Slices in Virtex-5 FPGA provides an added advantage of performing all math operations, relatively at a much higher speed.

Features

- Real time video processing
- Support 64 levels of Color adjustment
- Supports RGB 8:8:8 colour format
- Pixel by pixel processing
- Supports input resolution from QVGA (320 x 240) to SXGA (1280 x 1024)
- Optimized for Xilinx Virtex-5 FPGA

Applications

- In-Car Entertainment
- Image Processing
- Surveillance Systems
- Handheld Devices
- Medical Monitors
- Consumer Displays

Core Resource Utilization and Performance

Resource utilization after Place and Route in Virtex5 FPGA (XC5VSX50T-1FFG1136) is given in the table below.

Resource Type	Quantity Used
Slice Register	793
Slice LUT	334
Block RAM	5
DSP48E	24
Maximum Clock Frequency	250 MHz

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements using ModelSim and validated in Xilinx ML506 XtremeDSP development kit equipped with Virtex5 FPGA (XC5VSX50T-1FFG1136).

Standard Deliverables

- RTL source code in VHDL or post-synthesis EDIF/NGC netlist
- Sophisticated VHDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Product Datasheet
- Comprehensive User Guide with detailed application notes

Documentation

- Color Enhancer v1.0 Datasheet
- Color Enhancer v1.0 User Guide

Purchase and Technical Support

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